Electronic Version
Stylesheet Version v1.1.1

Description

[INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS]

Cross Reference to Related Applications

[0001] The present application is related to pending U.S. Patent Application 10/_____, filed concurrently herewith to Allen et al., entitled "CRITICAL AREA COMPOSITE FAULT MECHANISMS USING VORONOI DIAGRAMS" (IBM Docket No. BUR920030136US1). The foregoing application is assigned to the present assignee, and is incorporated herein by reference.

Background of Invention

[0002] Field of the Invention

[0003] The present invention generally relates to measuring critical area in integrated circuit design, and more particularly to a method that uses Voronoi diagrams to measure critical area as the design layout is changed.

[0004] Description of the Related Art

[0005] Within this application several publications are referenced by Arabic numerals within parentheses. Full citations for these, and other, publications may be found at the end of the specification immediately preceding the claims. The disclosures of all these publications in their entireties are hereby expressly incorporated by reference into the present application for the purposes of indicating the background of the present invention and illustrating the state of the art.

[0006] Advanced deep sub-micron technology enables millions of transistors to be fabricated on a single die. While this capability grants performance, the smaller size and higher density of layout features adversely affect yield [See: Papadopoulou, E., "Critical area computation for missing material defects in VLSI circuits ,"*Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* , Vol. 20, No. 5, pp 583-597, May 2001; Fook-Luen Heng and Zhan Chen. "VLSI Yield Enhancement Techniques Through Layout Modification."IBM T. J. Watson Research Center; and A. Venkataraman and I. Koren. "Trade-offs between Yield and Reliability Enhancement."*Proc. of the 1996 IEEE National Symposium on Defect and Fault Tolerance in VLSI Systems*, pp.

67-75, November 1996]. Both the manufacturing process and geometry of the layout contribute to this loss of yield.

[0007] A part of this yield loss comes from random defects. These defects occur during the manufacturing process and cause electrical faults when the chip is active. The types of electrical faults that may result include, but are not limited to, short-circuits, wire-breaks, and via obstructions. The probability of yield loss due to random defects relates to the critical area of the layout, which can be measured using a Voronoi diagram technique [See: Papadopoulou, E. and Lee, D.T., "Critical area computation via Voronoi diagrams,"*Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* , Vol. 18, No. 4, pp 463-474, April 1999].

[0008] Critical area of a very large scale integration (VLSI) layout is a measure that reflects the sensitivity of the layout to defects occurring during the manufacturing process. Critical area is widely used to predict the yield of a VLSI chip. Yield prediction is essential in today's VLSI manufacturing due to the growing need to control cost. Models for yield estimation are based on the concept of critical area which represents the main computational problem in the analysis of yield loss due to random (spot) defects during fabri-

cation. Spot defects are caused by particles such as dust and other contaminants in materials and equipment and are classified into two types: "extra material" defects causing shorts between different conducting regions and "missing material" defects causing open circuits.

[0009] In some defect modeling techniques, defects are modeled, consistently, as circles. The underlying reason for modeling defects as circles is the common use of Euclidean geometry. The distance between two points, usually, is measured by the length of the line segment joining the two points. This is the Euclidean distance. The locus of points a unit distance from a center point is usually called the "unit circle". In Euclidean geometry, the "unit circle" is a circle of radius one.

[0010] In reality, spot defects are not necessarily circular. They can have any kind of shape. Therefore, it seems appropriate to use other geometries if the critical area computation can be simplified by modeling defects as squares, diamonds or octagons. For practical purposes, a circular defect can certainly be approximated by a regular octagon. Yield estimation should not considerably depend on which of the above geometries is used to model defects as long as the geometry is chosen consistently. Therefore, the ge-

ometry used for a particular computation, preferably, should allow critical area computation in the most efficient way.

[0011] A Voronoi diagram can also be used to enhance the computation of critical area. A Voronoi diagram of a set of 2D geometric elements (polygons, line segments, points) is a partition of the plane into regions representing those points in the plane closest to a particular geometric element. Here, "closest"is defined in terms of an appropriate geometry as mentioned above. These regions are called Voronoi cells, each of which is associated with its defining geometric element, called the owner of the cell. The set of points which separates two Voronoi cells is called a Voronoi bisector. The point where three or more Voronoi bisectors (or Voronoi cells) meet is called a Voronoi vertex.

[0012] Based on the circuit design and under an appropriate geometry, Voronoi diagrams can be constructed to model the effect of extra-material and missing-material spot defects. The Voronoi diagram partitions the circuit design into Voronoi cells within which defects that occur cause electrical faults between the same two shape edges in the design. This information can then be used to compute

critical area. (e.g., see U.S. Patents 6,317,859, 6,247,853, and 6,178,539, which are incorporated herein by reference).

SUMMARY OF INVENTION

[0013] The invention provides a method of calculating critical area in an integrated circuit design. Starting with an initial integrated circuit design, the invention associates variables with the positions of the edges in the design. The invention associates cost functions involving the variables with the spacing among (between) these edges. The cost functions are in terms of critical area contributions. Critical area contributions comprise a measure of electrical fault characteristics of the spacing among edges. The invention optimizes the position and length of the edges to reduce critical area contribution cost in a first direction across the integrated circuit design to produce a revised integrated circuit design. Then, the invention optionally repeats this process with the revised integrated circuit design in a second direction to further reduce critical area contribution cost.

[0014] The process of associating cost functions maps points within the spacing among edges in the design to the size of defects at those points that trigger an electrical fault,

forming Voronoi cells. These Voronoi cells define Voronoi bisectors and Voronoi vertices which encode the variables associated with the edges. The invention defines cost functions based on these Voronoi elements but independent of their geometry. The cost function models critical area contributions of the edges in the design layout as they change position and length in a continuous manner.

[0015] These, and other, aspects and objects of the present invention will be better appreciated and understood when considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

Brief Description of Drawings

[0016] The invention will be better understood from the following detailed description with reference to the drawings, in which:

[0017] Figures 1A and 1B illustrate edges of design shapes and

the Voronoi bisectors that are created between the design shapes;

[0018] Figure 2 is a Voronoi cell in three dimensions;

[0019] Figure 3 is a diagram showing Voronoi bisectors;

[0020] Figure 4 is a diagram showing Voronoi bisectors;

[0021] Figure 5 is a diagram showing Voronoi bisectors;

[0022] Figures 6A-6C are diagrams showing Voronoi bisectors;

[0023] Figures 7A-7G are diagrams showing Voronoi bisectors;

[0024] Figure 8 is a flow diagram illustrating processing according to the invention;

[0025] Figures 9A-9C illustrate bisectors, and graphical cost functions associated with bisectors;

[0026] Figures 10A-10C illustrate bisectors, and graphical cost functions associated with bisectors;

[0027] Figures 11A-11C illustrate bisectors, and graphical cost functions associated with bisectors;

[0028] Figures 12A-12C illustrate bisectors, and graphical cost functions associated with bisectors;

[0029] Figures 13A-13C illustrate bisectors, and graphical cost functions associated with bisectors;

[0030] Figures 14A-14C illustrate bisectors, and graphical cost

functions associated with bisectors;

[0031] Figures 15A-15C illustrate bisectors, and graphical cost functions associated with bisectors;

[0032] Figures 16A-16C illustrate bisectors, and graphical cost functions associated with bisectors;

[0033] Figures 17A-17C illustrate bisectors, and graphical cost functions associated with bisectors;

[0034] Figures 18A-18C illustrate bisectors, and graphical cost functions associated with bisectors;

[0035] Figures 19A-19C illustrate bisectors, and graphical cost functions associated with bisectors;

[0036] Figures 20A-20C illustrate bisectors, and graphical cost functions associated with bisectors;

[0037] Figures 21A-21C illustrate bisectors, and graphical cost functions associated with bisectors;

[0038] Figures 22A-22C illustrate bisectors, and graphical cost functions associated with bisectors;

[0039] Figures 23A-23C illustrate bisectors, and graphical cost functions associated with bisectors;

[0040] Figures 24A-24C illustrate bisectors, and graphical cost functions associated with bisectors;

[0041] Figures 25A-25C illustrate bisectors, and graphical cost functions associated with bisectors;

[0042] Figures 26A-26C illustrate bisectors, and graphical cost functions associated with bisectors;

[0043] Figures 27A-27C illustrate bisectors, and graphical cost functions associated with bisectors;

[0044] Figures 28A-28C illustrate bisectors, and graphical cost functions associated with bisectors;

[0045] Figures 29A-29C illustrate bisectors, and graphical cost functions associated with bisectors;

[0046] Figures 30A-30C illustrate bisectors, and graphical cost functions associated with bisectors;

[0047] Figures 31A-31C illustrate bisectors, and graphical cost functions associated with bisectors;

[0048] Figures 32A-32C illustrate bisectors, and graphical cost functions associated with bisectors;

[0049] Figure 33 illustrates Voronoi bisectors;

[0050] Figure 34 illustrates Voronoi bisectors;

[0051] Figure 35 illustrates Voronoi bisectors; and

[0052] Figure 36 is a hardware embodiment in which the invention can operate.

DETAILED DESCRIPTION

[0053] The present invention and the various features and advantageous details thereof are explained more fully with

reference to the non-limiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0054] First, the invention constructs a weighted Voronoi diagram (shown in Figures 1A and 1B) for a particular electrical fault mechanism using known techniques. Denote this as *Voronoi (fault)*. Electrical fault mechanisms are defined by the type of defect that may occur and one or more levels in the design involved in the fault. The Voronoi diagram that results maps points in the involved layout levels to their distance from edges of device shapes triggering the electrical fault (shown by the arrows in Figure 1B). This Voronoi diagram partitions the layout into Voronoi cells 110, or sets of contiguous points which share common

fault-triggering edges 118 of a device shape 116. The boundaries 112 between cells 110 are known as Voronoi bisectors 112. The points where two or more Voronoi bisectors 112 meet are known as Voronoi vertices 114.

[0055] A visualization of the mapping provided by *Voronoi (fault)* is that of a three-dimensional surface (e.g., see Figure 2). Imagine the layout design to be on the x-y plane and let the z-axis represent the mapped distance. The use of squares to model the shape of defects [1] results in Voronoi cells 110 that are piece-wise defined planar surfaces, and bisectors 112 that are linear. This three-dimensional surface can be described by some planar, piece-wise continuous function over the positions and orientation of the bisectors 112 in the layout.

[0056] Critical area represents the likelihood of a random defect and is a function over the surface the Voronoi diagram represents. The critical area within *Voronoi (fault)* is the sum of the critical areas contributions of its cells 110. Furthermore, the critical area contribution of each cell can be computed as the sum of the critical area contribution of the bisectors bordering the cell. This is achieved using a trapezoidal decomposition technique. This is achieved using a trapezoidal decomposition technique (as described

in reference [1])The goal of yield improvement here is to reduce the critical area within the layout. While *Voronoi (fault)* allows us to compute the current critical area, it does not describe how critical area changes as a result of layout modification. In the following sections, a set of cost functions are presented which describe critical area in terms of variables representing the positions of edges 118 in the design. This enables one to compute critical area as the edges 118 in the design change. This in turn enables one to optimize the geometry of the edges 118 in the design to reduce critical area and, thus, improve yield.

[0057] Let K represent an edge 118 in the design as shown in Figure 2.

$$\text{Let } \vec{x}_K = \langle x_K, y_K, 0 \rangle \text{ represent a point } \langle x_K, y_K \rangle \text{ on K.}$$

$$\text{Let } \vec{g}_K = \langle g_{Kx}, g_{Ky} \rangle \text{ represent the gradient of K.}$$

[0058] The gradient of K is the direction of increasing distance from K. The gradient is perpendicular to the orientation of K in the L-infinity distance metric, for all possible orientations. Its magnitude is arbitrarily but consistently chosen.

[0059] For the rectilinear boundary around the entire layout design, we define special gradients as follows.

$$\vec{g}_{\text{horizontal boundary}} = \beta_{\langle 0,1\rangle} \qquad \vec{g}_{\text{vertical boundary}} = \beta_{\langle 1,0\rangle}$$

Let $\vec{n}_K = \langle n_{Kx}, n_{Ky}, n_{Kz} \rangle$ represent the normal vector of the plane in three-dimensions representing distance away from K. For the L-infinity distance metric,

$$\vec{n}_K = \begin{cases} \langle -g_{Kx}, -g_{Ky}, |g_{Kx}| + |g_{Ky}| \rangle & \vec{g}_K \notin \{\beta_{\langle 1,0\rangle}, \beta_{\langle 0,1\rangle}\} \\ \langle 1,0,0 \rangle & \vec{g}_K = \beta_{\langle 1,0\rangle} \\ \langle 0,1,0 \rangle & \vec{g}_K = \beta_{\langle 0,1\rangle} \end{cases}$$

[0060] In other words, this portion of the disclosure defines the normal vector that is based on the orientation (encoded in the gradient) of the edges in the design. It shall be used to represent the mapping described by Voronoi cells in a way that is independent of the geometry comprising the Voronoi diagram itself. This can then be used to formulate cost functions to calculate the critical area contribution of the various edges of shapes within the integrated circuit design subject to modification and avoids the need to re-construct the Voronoi diagram under these modifications.

[0061] As shown in Figure 3, Vertex (A, B, C) 114 represents the coordinate of a Voronoi vertex defined by edges A, B, and C of device shapes 116 in the design. This coordinate can be defined based on, but independent of, Voronoi vertices in the Voronoi diagram. Note that the devices, Voronoi bi-

sectors, Voronoi vertices, etc. are not explicitly identified in all the drawings, so as to simplify the drawings and direct the reader's attention to the salient portions of the invention.

$$\text{Vertex (A, B, C)} = \frac{(\vec{x}_A \bullet \vec{n}_A)(\vec{n}_B \times \vec{n}_C) + (\vec{x}_B \bullet n_B)(\vec{n}_C \times \vec{n}_A) + (\vec{x}_C \bullet \vec{n}_C)(\vec{n}_A \times \vec{n}_B)}{Det[\vec{n}_A \quad \vec{n}_B \quad \vec{n}_C]}$$

[0062] • represents the dot-product operator

[0063] x represents the cross-product operator

[0064] In other words, the coordinate of the vertex is a function of variables representing the positions and orientations (encoded as normals) associated with the involved edges in the design. This formulation is that of the intersection of the planes (as mentioned earlier) defined by the involved edges in the design.

[0065] As shown in Figure 4, Bisector (A, B, C, D) 112 represents a Voronoi bisector whose geometry is defined by edges A, B, C, D of device shapes 116 in the design. These edges are stated in clockwise order around the bisector, such that B and D are on either side of the bisector. By definition, Bisector (A, B, C, D) it is a line segment between vertices 114 *Vertex (A, B, D)* and *Vertex (B, C, D)*.Let Contribution (Bisector (A, B, C, D) represent the critical area contribu-

tion associated with a Voronoi bisector defined by edges A, B, C, and D in the design. Using squares to model the shape of defects, applying a trapezoidal decomposition technique (as described in Papadopoulou, E. and Lee, D.T., "Critical area computation via Voronoi diagrams,"*Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* , Vol. 18, No. 4, pp 463-474, April 1999.), and applying the equations derived above, critical area contribution is given by

$$Contribution\left(Bisector\left(A,B,C,D\right)\right)=$$

$$\kappa\left(NormalXY\left(B\right)-NormalXY\left(D\right)\right)\times\left(\frac{Vertex\left(C,B,D\right)_{xy}-Vertex\left(A,B,D\right)_{xy}}{Vertex\left(C,B,D\right)_{z}-Vertex\left(A,B,D\right)_{z}}\ln\frac{Vertex\left(C,B,D\right)_{z}}{Vertex\left(A,B,D\right)_{z}}\right)$$

where κ is a constant and

$$NormalXY\left(K\right)=\frac{n_{Kz}}{\vec{n}_{Kxy}^{2}}\vec{n}_{Kxy}$$

and for any vector $\vec{r}=\langle x,y,z\rangle$,

$$\vec{r}_{xy}=\langle x,y\rangle$$
$$r_{z}=z$$

[0066] In other words, the critical area contribution of a Voronoi bisector is a function of the orientation (encoded as normals) and positions of edges in the design. The critical area contribution of each Voronoi bisector is proportional to the cross product of two vectors the x-y difference vector between the normal vectors of the planes which meet at the bisector, and the x-y difference vector repre-

senting the length of the bisector. The factor of proportionality is some constant times the logarithm of the z-coordinates of the vertices of the bisector divided by the difference in the z-coordinates of the vertices of the bisector.

[0067] This equation is valid until the bisector or an adjacent bisector collapses to zero-length, resulting in a topological change in the Voronoi diagram. Having expressed the critical area contribution of a Voronoi bisector as a function of edges in the design enables the invention to predict change in critical areas as a result of layout modification. Based on the properties of the Voronoi diagram, the following observations can be made. Under continuous layout modification, the vertices in the Voronoi diagram shift positions predictably; the three-dimensional surface the Voronoi diagram represents changes in a continuous manner; the critical area of the layout changes continuously since it is a continuous function over this three dimensional surface; and when such motion causes a Voronoi bisector to collapse to zero-length, its critical area contribution converges to zero:

$$\lim_{Vertex(C,B,D)\to Vertex(A,B,D)} Contribution\left(Bisector\left(A,B,C,D\right)\right)=0$$

[0068] A further observation is that the point at which a bisector collapses is a function of the involved edges in the design. In fact, it is the point at which the coordinates of the two vertices defining the bisector converge. Therefore, one can predict the state in which a particular critical area contribution equation is valid under continuous modification of edges in the design. Furthermore, after collapse, an expansion may occur when modification continues, resulting in the emergence of a new bisector with a critical area contribution. This transformation is predictable and stated as follows (see Figure 5).

$$Bisector(A,B,C,D) \xrightarrow{\|Vertex(C,B,D)-Vertex(A,B,D)\|=0} Bisector(D,A,B,C)$$
$$Bisector(A,B,C,D) \xrightarrow{\|Vertex(E,B,A)-Vertex(D,B,A)\|=0} Bisector(E,B,C,D)$$
$$Bisector(A,B,C,D) \xrightarrow{\|Vertex(F,A,D)-Vertex(B,A,D)\|=0} Bisector(F,B,C,D)$$
$$Bisector(A,B,C,D) \xrightarrow{\|Vertex(D,B,C)-Vertex(G,B,C)\|=0} Bisector(A,B,G,D)$$
$$Bisector(A,B,C,D) \xrightarrow{\|Vertex(B,C,D)-Vertex(H,C,D)\|=0} Bisector(A,B,H,D)$$

[0069] As illustrated, when Bisector (A, B, C, D) or a bisector adjacent to Bisector (A, B, C, D) in the Voronoi diagram collapses, a new bisector replaces Bisector (A, B, C, D). For example, suppose Vertex (B, C, D) and Vertex (H, C, D) are the first to converge. After convergence, Bisector (A, B, C, D) is replaced with Bisector (A, B, H, D) and therefore, Contribution (Bisector (A, B, C, D)) is replaced by Contri-

bution (Bisector (A, B, H, D).

[0070] Note that the identification of the device shapes, etc. has been intentionally omitted from Figure 5 to more clearly illustrate the invention, as mentioned above. The replacement of one vertex for another is shown in the following transformations.

[0071] For a Bisector (A, B, C, D) shown in Figure 5 the critical area cost function is stated as follows.

$$Cost\left(Bisector\left(A,B,C,D\right)\right)=\begin{cases} Contribution\left(Bisector\left(A,B,C,D\right)\right) & \text{Space I} \\ \varepsilon Contribution\left(Bisector\left(A,B,C,D\right)\right) & \text{Space II} \end{cases}$$

[0072] Contribution accurately describes the critical area contribution of the Voronoi bisector within Space I. This is the space in which the edges in the design start. Space II is the space of variables in which Contribution no longer accurately describes the critical area contribution of the Voronoi bisector due to a collapse of the bisector or of an adjacent bisector. These two spaces are separated by a multi-dimensional surface defined by

$$\|Vertex(C,B,D) - Vertex(A,B,D)\| = 0$$
$$\|Vertex(E,B,A) - Vertex(D,B,A)\| = 0$$
$$\|Vertex(F,A,D) - Vertex(B,A,D)\| = 0$$
$$\|Vertex(D,B,C) - Vertex(G,B,C)\| = 0$$
$$\|Vertex(B,C,D) - Vertex(H,C,D)\| = 0$$

[0073] where E, F, G, and H are those edges in the design relating to bisectors adjacent to Bisector (A, B, C, D) as in the earlier discussion. In the case where one accounts for topological change through the transformations previously described, the value of ϵ should be set to zero. Otherwise, the invention chooses a value ϵ with which to penalize the cost function within Space II. By this technique, it confines the cost function to variables associated with only four edges at a time within the design.

[0074] In other words, instead of statically calculating critical area contribution from a Voronoi diagram, the invention utilizes a plane normal to represent each Voronoi cell defined by various device edges in the integrated circuit design. Using these normals to calculate the Voronoi bisectors allows the invention to develop a cost function in terms of variables associated with the positions of device edges, independent of the Voronoi diagram itself. There-

fore, when the positions of the device edges change, the values of each of the vertex coordinates will also change in accordance, thereby altering the critical area contribution. By presenting the critical area contribution as a cost function, the invention allows an optimization process to reduce the critical area contribution cost.

[0075] The invention associates this cost function with every Voronoi bisector Bisector (A, B, C, D) in the diagram. To extend the range of predictability, one can also associate cost functions with the possible transformations of Bisector (A, B, C, D) described by the previous section.

[0076] The critical area minimization objective is, therefore,

$$Objective: Minimize$$
$$\sum_{fault} \sum_{Bisector\ B \in Voronoi(fault)} \sum_{Bisector(A,B,C,D) \in B \cup \text{transformations of } B} Cost\left(Bisector\left(A,B,C,D\right)\right)$$

[0077] In other words, the invention minimizes the sum of all costs from all bisectors, and transformations thereof (subject to constraints such as topological and ground-rule constraints), for every fault mechanism in the integrated circuit design.

[0078] A non-linear, multi-dimensional optimization algorithm may be used to solve the foregoing objective for the positions of all movable edges in the layout. Such algorithms are NP-complete or stochastic. Fortunately, there are a

few simplifications that can be made to the cost function that would enable the use of a linear optimization algorithm, which is considerably more efficient.

[0079] Let a, b, c, d, be some constants. Let w represent the sum or difference of two variables; the set of variables being the x and y coordinate of all movable edges in the layout. Without loss of generality, apply the following simplifications. The example used herein assume orthogonal data, however, one ordinarily skilled would understand that any arbitrary angles could be used.

[0080] I. Restrict the set of variables to represent a single dimensional movement (other dimensions may be handled using various techniques, for example, constraining them to move with an adjacent orthogonal edge.) Then

$$\vec{g}_K \in \left\{\langle -1,0\rangle, \langle 1,0\rangle, \langle 0,-1\rangle, \langle 0,1\rangle, \beta_{\langle 1,0\rangle}, \beta_{\langle 0,1\rangle}\right\}$$
$$\vec{n}_K \in \left\{\langle 1,0,1\rangle, \langle -1,0,1\rangle, \langle 0,1,1\rangle, \langle 0,-1,1\rangle, \langle 1,0,0\rangle, \langle 0,1,0\rangle\right\}$$

[0081] The critical area contribution of a Voronoi bisector simplifies to

$$Contribution\left(Bisector\left(A,B,C,D\right)\right) \in \left\{a\frac{w_1}{w_2}+b,\ a\ln\frac{w_1}{w_2}+b\right\}$$

[0082] II. Ignore the effect of adjacent Voronoi bisectors collaps-

ing and consider only the Voronoi bisector itself collapsing. Then the condition at which Contribution is no longer accurate can be expressed by

$$cw_1 + dw_2 = 0$$

[0083] III. Solve the objective in two passes. In the first pass, consider only those variables which represent x-coordinates. In the second pass, consider only those variables which represent y-coordinates. Then

$$Contribution\left(Bisector\left(A,B,C,D\right)\right) \in \left\{aw+b,\ \frac{a}{w}+b,\ a\ln w+b,\ a\ln w_1+b\ln w_2\right\}$$

[0084] IV. Approximate Contribution using a piecewise-linear function.

[0085] Actions I and II result in a cost function over sums or differences of variables. Actions III and IV result in cost functions that are convex and piecewise-linear. An efficient optimization algorithm such as graph-based simplex can then be applied.

[0086] In other words, allowing edges to move along a single axis (x-axis or y-axis) simplifies the cost function and enables it to be used within a linear optimization algorithm which is considerably more efficient that a general optimization algorithm.

[0087] There are a number of topologies that may exist within the Voronoi diagram which are not handled by the above cost function. These fall into one of two categories ambiguities and degeneracies. Ambiguities shall now be addressed.

[0088] An ambiguity is present when the plane normals on either side of a Voronoi bisector are parallel to each other as shown in Figure 6A. For example,

$Bisector(\{P,Q\},B,C,D)$ may have the property that $\bar{g}_B = \bar{g}_D$ and, consequently, $\vec{n}_B = \vec{n}_D$. Functions $Vertex(\{P,Q\},B,D)$ and $Vertex(C,B,D)$ are only applicable when P, Q, B, D and C, B, D have non-parallel plane normals. For orthogonal data, modification to bisectors B and D may result in one of two scenarios shown in Figures 6B and 6C where a Voronoi cell emerges at the bisector.

[0089] To account for such changes, the following decomposition can be used

$$Bisector(\{P,Q\},B,C,D) \rightarrow \begin{Bmatrix} Bisector(Q,P,C,D), Bisector(D,P,B,C), \\ Bisector(P,B,C,Q), Bisector(D,Q,B,C) \end{Bmatrix}$$

where $\bar{g}_P \neq \bar{g}_Q, \bar{g}_P \perp \bar{g}_B$, and $\bar{g}_Q \perp \bar{g}_B$.

[0090] In a scenario such as this, where one accounts for topological change, the value ϵ in the cost functions associated with bisectors resulting from the decomposition should be set to zero.

[0091] In other words, when a bisector is encountered with ambi-

guity, the invention decomposes the bisector to its potential forms during layout modification, resulting in unambiguous bisectors. This rule may be applied iteratively until no ambiguities are present. A cost function is then derived for every Voronoi bisector at the end of the decomposition. Under layout modification the cells 110 that emerge are initially of zero area and contribute no critical area to that of the overall layout. If one scenario becomes dominant, its associated cost functions will assert themselves within the space of predictability while those of the other scenarios are suppressed as a consequence of being outside the space of predictability. The overall effect is an accurate modeling of how critical area will change under layout modification in cases of ambiguity.

[0092] As mentioned above, there are a number of topologies that may exist within the Voronoi diagram which are not handled by the cost function and these fall into one of two categories ambiguities and degeneracies. Degeneracies shall now be addressed.

[0093] A degeneracy is present when more than three bisectors converge at a single Voronoi vertex, as shown in Figure 7A. Modification to the layout may result in an emergence of one or more bisectors at this vertex, as shown in Fig-

ures 7B-7G. In other words, the invention decomposes these vertices into all possible scenarios that may result under layout modification, resulting in additional vertices and bisectors. Figures 7B-7G illustrate the different possibilities that can occur from Figure 7A under layout modification. Thus, for every subset of four edges in the design defining the Voronoi vertex, the invention applies the following decomposition.

$$Vertex(\{A,B,C,D\}) \rightarrow \{Bisector(A,B,C,D), Bisector(B,C,D,A)\}$$

[0094] Additionally, the invention derives a cost function for every Voronoi bisector resultant from this decomposition. The Voronoi bisectors in this decomposition initially have zero-length and their critical area contribution is zero. As the bisectors grow in length, their cost functions move into the space of predictability and dominate those associated with Voronoi bisectors that do no emerge. In a scenario such as this, where one accounts for topological change, the value ϵ in the cost functions associated with bisectors resulting from the decomposition should be set to zero. The overall effect is an accurate modeling of how critical area will change under layout modification in cases of degeneracy.

[0095] Figure 8 illustrates the flow for yield improvement using the critical area minimization objectives. More specifically, in item 800, the invention inputs an initial layout. For every applicable fault mechanism (parameterized by type of defect and the involved layout levels), the invention builds layout variables for movement in one axial direction (as shown in item 802). More specifically, the invention associates variables to the positional components of the edges that lie in a first direction in the initial integrated circuit design. Then, in item 804, the invention constructs Voronoi diagrams. The creation of these Voronoi diagrams occurs incrementally as processing moves across the integrated circuit design. As each Voronoi bisector is finalized, processing moves to item 806 which decomposes the bisector (eliminates ambiguity or degeneracy as discussed above).

[0096] Once each Voronoi bisector is decomposed, the invention associates a cost function in terms of critical area contributions of the Voronoi bisectors in item 808. As shown above, this cost function is a function of the positions and orientations (encoded as normals) of the edges, and the critical area contributions comprise a measure of electrical fault characteristics of the areas between the edges.

[0097] In items 810, the invention applies a linear optimization algorithm to all the cost functions that are collected from item 808 and processing optionally returns to item 800 to optimize for another axis (orthogonal, or any other useful direction (45 degrees, 60 degrees, etc.)). Thus, the invention optimizes the positions and length of the edges to reduce critical area contribution cost in the first direction across the integrated circuit design to produce a revised integrated circuit design and then, the invention repeats this process with the revised integrated circuit design in a different direction.

[0098] In a standard run, optimization is performed twice, once along each of the x and y axes. For further yield improvement, more iterations of this flow can be executed. This flow may be combined with the generation of other cost functions and objectives such as topological or ground-rule constraints and objectives. When combining multiple objectives, each should be weighted appropriately relative to each other.

[0099] Figures 9A-32C illustrate some possible Voronoi bisector configurations. More specifically, the "A" Figures (of Figures 9A-32C) illustrate the specific Voronoi bisector configuration and the appropriate cost functions for such

Voronoi bisector configuration. In the "A" Figures, the arrows represent the direction of gradient. The "B" Figures (of Figures 9A-32C) illustrate the graphical results of the cost function in one direction and the "C" Figures (of Figures 9A-32C) illustrate the graphical results of the cost function in a direction orthogonal to the first direction. The illustrated cost functions also apply to configurations that are rotationally or reflectively symmetric to the drawn configuration.

[0100] Figures 33-35 represent Voronoi bisector configurations which do not contribute a cost function to the optimization algorithm because modifications of the involved variables do not change their critical area contributions. For this reason, they are ignored and not included within the total of all cost functions (item 808).

[0101] A representative hardware environment for practicing the present invention is depicted in Figure 36, which illustrates a typical hardware configuration of an information handling/computer system in accordance with the subject invention, having at least one processor or central processing unit (CPU) 10. CPUs 10 are interconnected via system bus 12 to random access memory (RAM) 14, read-only memory (ROM) 16, an input/output (I/O) adapter 18

for connecting peripheral devices, such as disk units 11 and tape drives 13, to bus 12, user interface adapter 19 for connecting keyboard 15, mouse 17, speaker 103, microphone 104, and/or other user interface devices such as touch screen device (not shown) to bus 12, communication adapter 105 for connecting the information handling system to a data processing network, and display adapter 101 for connecting bus 12 to display device 102. A program storage device readable by the disk or tape units, is used to load the instructions which operate the invention also loaded onto the computer system.

[0102] Therefore, as shown above, the invention presents a method, system, program storage device, etc. that calculates and reduces critical area in an integrated circuit design. More specifically, the invention begins with an integrated circuit design as its initial input. It associates variables with the positions of edges in the integrated circuit design. It encodes the orientation of edges in the integrated circuit design as normals.

[0103] The invention defines cost functions of these variables in terms of the critical area contributions within the spacings for the edges associated with these variables. The critical area contributions comprise a measure of the electrical

characteristics of the integrated circuit for a particular type of fault.

[0104] The invention associates cost functions of these variables with particular spacings among particular edges in the design. This process uses a three-dimensional representation of the Voronoi diagram constructed for the integrated circuit design for a particular type of electrical fault. In this process, the invention defines Voronoi cells as a mapping of points in the spacing between edges in the design to the minimum size of defects that trigger an electrical fault between them. The set of points where Voronoi cells meet define Voronoi bisectors. The endpoints of these bisectors form Voronoi vertices.

[0105] The invention represents Voronoi cells, bisectors, and vertices using mathematical expressions, independent of the Voronoi diagram itself, over the variables associated with the edges of the integrated circuit design involved in the spacing. Based on these entities, the invention formulates cost functions which describe the critical area contributions of the spacing under continuous modification of the design.

[0106] The invention uses these cost functions in an optimization algorithm to modify the positions and length of the edges

in the integrated circuit design to reduce critical area contribution cost. For improved efficiency with a linear optimization algorithm, the invention applies the optimization for variables in one direction across the integrated circuit design to produce a revised integrated circuit design. The invention optionally repeats this process using the revised integrated circuit design in another direction to further reduce critical area cost.

[0107] As we enable ourselves to build smaller and denser integrated circuits, their sensitivity to the occurrence of spot defects inherent in the manufacturing process becomes of greater importance. Such defects cause electrical faults within the circuit, contribute to yield loss, and ultimately result in lost resources. This invention addresses the problem by providing an automated means of optimizing a circuit design to reduce this sensitivity. Furthermore, the process described herein can be combined with other optimization objectives to achieve a balance of costs in the modified design.

[0108] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.